ELLIOTT 900

Volume 4: ENGINEERING MAINTENANCE

Part 3: OPTIONAL UNITS

Section 1: MULTIPLEXER (DPA 312, 314, 316, 318)

CONTENTS

March, 1968. (Issue 3)

END-OF-TEXT FIGURES

Printed in England by
Engineering Unit, Elliott-Automation Computers Ltd.

Chapter 1: GENERAL DESCRIPTION

1.1 Introduction

The multiplexer is used by the 900 central processor to enable the processor to be connected to a large number of peripherals. The multiplexer is an expanding interface connection which receives control, address, output and input data from the processor and fans out the information to a maximum of 8 channels. Other multiplexers may be connected to the outputs of any channel, thus further expansion is possible. A facility is also provided on the multiplexer to enable the processor to select Group B (channels 1 and 2), Group A (channels 3 and 4) or Groups A and B (channels 1 to 4 inclusive).

The multiplexer, which can be located in half a standard cabinet, is a self-contained unit on three shelves (see Figure 1). The top shelf contains the plug-in boards (18), the middle shelf the plugs and sockets and the bottom shelf the two power supplies (three if the NPL Interface is in the same cabinet).

1.2 Channel Selection

There are three methods of selecting channels on the multiplexer. The first two methods enable the processor to select channels 1 and 2 (GROUP B selected), Channels 3 and 4 (GROUP A selected) or Channels 1, 2, 3 and 4 (GROUPS A & B selected). The third method of selecting channels (channels 5 to 8 inclusive) is by the addition of logic boards 12 to 19 inclusive (see Figure 5).

If the control logic board (DP30) is removed the processor can no longer select channels and the multiplexer becomes an expanding connection with all signals going straight through the connection.

1.3 Control, Address, Output and Input Data

There are eight control signals received by the multiplexer, 4 from the processor (SOP, SIP, BT and LW) and 4 from the peripherals (PI1, PI2, PI3 and PR). Signal LW goes straight through the multiplexer but signals SOP, SIP and BT are gated and diverted to the selected group of channels. The signals from the peripherals are received and transmitted directly to the processor.

Eleven address lines, RESET and 18 Output data (OA) signals are received from the processor and are transmitted via all channels to the peripherals. Six of the address lines are also used with RESET and SOP for channel selection and reset.

Eighteen Input data (IG) signals from the peripherals are received by the multiplexer and transmitted to the processor.

All control lines, using coaxial cables, are on PL13 (from and to processor) and SK13 (to and from peripherals). All data lines, using ordinary cableforms, are on PL4 (from and to processor) and SK4 (to and from peripherals).

1.4 Additional Multiplexers

Additional multiplexers may be used to increase the fan-out by connecting them to any channel output socket of the previous multiplexer; thus a large number of peripherals may be connected to the processor via the multiplexer.

1.5 Power Supplies

There are two power supplies, +6 V and -6 V located on the bottom shelf of the multiplexer. These supplies are switched on by plugging in the mains plug.

If a NPL Interface shares the same cabinet as the multiplexer the NPL power supply is also positioned on the multiplexer power supply shelf.

Chapter 2: LOGIC DESCRIPTION

2.1 Introduction

The logic used on the multiplexer is NAND type and the elements for the logic are Logic Sub-Assemblies (LSA elements, see Section 4.6.1.).

The signals to and from the processor and multiplexer are enclosed in square brackets [ ] and all signals to and from the peripherals and multiplexer are enclosed in diamond brackets < >. In the logic diagram where identical boards are used for different purposes, the second use of the board is in round brackets ( ). All discrete components, not being part of sub-assemblies, are fitted in Area G in the logic board. In the logic diagrams the IG inputs and all outputs are written in the form SK/CH/pin,

thus 4/1/Y is interpreted as SK4, any odd channel (1, 3, 5 or 7) and pin Y

while 4/2/X is interpreted as SK4, any even channel (2, 4, 6 or 8) and pin X.

As the system can comprise of from 2 to a maximum of 8 channels, only the number of channels required are provided and the positions for the unused channels are replaced by blank panels. The logic boards for the channels not being used are also removed.

Figure 5 gives a general breakdown of the system in block diagram form and shows all the LSA elements used, their area on the DP board, details of discrete components and the positions occupied by the logic boards in the 2-, 4-, 6- and 8-channel mutliplexers.

2.2 Channel Selection (Figure 3)

Channel selection is divided into two Groups A and B. If Group B or A is set to true then channels 1 and 2 or 3 and 4 are selected respectively. When Groups A and B are set to true then channels 1 to 8 are selected if all the logic boards are inserted in the rack. To select only four or six channels the appropriate boards shown in Figure 5 are plugged in.

When no control instructions are received on the multiplexer the $\overline{PR}$ bistable is true and [PR] is reset to false. On receiving the address, OS8, 9, 10 and 11 with SOP, a 470 ns pulse generator is triggered. The output of the pulse generator after three inversions reset $\overline{RS}$ to false. When $\overline{RS}$ is false the GA (Group A) and GB (Group B) bistables are reset. The output of the 470 ns pulse generator going false triggers a 330 ns pulse generator which sets the term SS1 to true. SS1 is gated with address bits OS2 or OS1 and when an address or both addresses are selected then the appropriate GB, GA or GB and GA bistables are set. On SS1 going false another pulse generator is triggered which with OS8, 9, 10, 11 and SOP set to true will reset the $\overline{PR}$ bistable to false and set [PR] to true. The $\overline{PR}$ bistable is set to true when SOP is reset to false.

When the processor sends [RESET] then $\overline{RESET}$* goes false sets the GA and GB bistables to true. With GA and GB true all channels are selected.

When GB is set to true control signals SOP, SIP and BT are allowed to be transmitted to channels 1 and 2 on board DP31 location 3. When GA is set to true signals SOP, SIP and BT are permitted to be transmitted to channels 3 and 4 on board DP32 location 4, channels 5 and 6 on board DP36 location 12 and channels 7 and 8 on board DP36 location 13 (see Figure 5). Control signals will only be transmitted to channels 5 to 8 inclusive if their respective boards (see Figure 5) are inserted in the appropriate locations.

Chapter 3: POWER SUPPLIES

3.1 Introduction

There are two power supplies, +6 V and -6 V, on the bottom shelf of the multiplexer. As these supplies are proprietary items literature is provided for them by the manufacturer. Also situated on the bottom shelf is a filter and an over-voltage and under-voltage protection circuit (Figures 1 and 2).

3.2 Inter-Connection of Supplies

The two supplies are connected together such that the negative of the +6 V is commoned to the positive of the -6 V and the common point is linked to the Earth busbar. The supply potentials are then taken to the following pins on the logic boards:-

(a) +6 V to pins 2, 31, 34 and 63 (Cat.No. 11186)

(b) -6 V to pins 3 and 35 (Cat.No. 11258)

(c) Earth busbar to pins 1, 32, 33 and 64.

3.3 Earths

The coaxial cable screen connections on PL13 and SK13 are connected to the following pins and then to the Earth busbar:-

PI1 screen to pin B	SIP screen to pin K
PI2 screen to pin D	PR screen to pin M
PI3 screen to pin F	BT screen to pin P
SOP screen to pin H	LW screen to pin S